REMARKS

Examiner Interview

Applicant acknowledges with appreciation the courtesy of a telephone interview extended by Examiner Ly D. Pham to Applicant's agent, Lois D. Cartier, on January 14, 2005. During the interview, no exhibit was shown and no demonstration was conducted. Claims 1-4 were discussed. It was agreed that Applicant would submit the above amendments, and that the above amendments are sufficient to overcome the present rejections.

Applicant acknowledges with gratitude the Examiner's courtesy and helpfulness during this telephone interview.

Initialed Form PTO-1449 Not Provided to Applicants

Applicant submitted along with the initial filing of the present application on February 26, 2004 a Substitute Form PTO-1449 bringing certain references to the attention of the Examiner.

The MPEP states:

> The examiner must consider all citations submitted in conformance with the rules and this section, and their initials when placed adjacent to the considered citations on the list or in the boxes provides a clear record of which citations have been considered by the Office.... If any of the citations are considered, a copy of the submitted list, form PTO-1449, or PTO/SB/08A and 08B, as reviewed by the examiner, will be returned to the applicant with the next communication.
> MPEP 609 III C(2)

Applicant did not receive an initialed copy of this form with the Office Action mailed October 27, 2004.

Applicant respectfully requests that a copy of the initialed form be provided to Applicant. The copy can be included with the next communication from the Patent Office regarding the present application, or can be sent to Applicant's agent via facsimile at the following number: 408-377-6137.

Supplemental Information Disclosure Statement

Applicant respectfully draws the Examiner's attention to the Supplemental Information Disclosure Statement filed herewith.

Summary of Claim Status

Claims 1 and 3-4 are pending in the present application after entry of the present amendment. Claims 1–4 are rejected for the reasons discussed below.

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the present amendment and in light of the following remarks.

Rejections for Double-Patenting

Claims 1-4 are rejected under the doctrine of obviousness-type double patenting over U.S. Patent No. 6,735,110. In response, Applicant has enclosed herewith a terminal disclaimer for the present invention with respect to the cited patent.

Rejections Under 35 USC 112

Claims 1-4 are rejected as being indefinite under 35 USC 112, the Office Action stating:

> In **claim 1**, lines 13-18, the limitation '...first and second transistors programmable to provide low and high resistances... is considered vague and indefinite since it is not clear to one of ordinary skill in the art what values of the resistances are considered low, or high. [*emphasis original*]

Applicant has amended Claim 1 to recite "a low resistance less than 1000 ohms and a high resistance of more than 100,000 ohms". Thus, this rejection is believed to be overcome.

Support for this amendment is found, for example, in paragraph 0008 of the specification as filed. Therefore, no new matter is added.

Rejections Under 35 USC 102(e)

Claims 1-2 are rejected as being anticipated by Golke et al. (U.S. Patent No. 6,058,041, hereinafter Golke). Applicant has amended Claim 1 to recite:

> 1. A memory device having single event upset resistant circuitry, comprising:
> a first inverter having a first input node and a first output node;
> a second inverter having a second input node and a second output node;
> a first transistor having a first source/drain contact coupled to the first input node and a second source/drain contact coupled to the second output node; and
> a second transistor having a third source/drain contact coupled to the second input node and a fourth source/drain contact coupled to the first output node,
> wherein each of the first and second transistors is programmable to provide a low resistance less than 1000 ohms and a high resistance of more than 100,000 ohms,
> wherein each of the first and second transistors has a gate coupled to a gate bias voltage source, the gate bias voltage source putting the first and second transistors into a partially conductive state to provide the high resistances,
> wherein the first and second transistors each have floating bodies, and
> wherein the first transistor and the second transistor each have a body contact coupled to a body bias source voltage.

As amended, Claim 1 is believed to distinguish over the cited references. Claim 2 is cancelled as being redundant with amended Claim 1.

This amendment is supported at least by paragraph 0027 of the application as filed. Therefore, no new matter is added.

Rejections Under 35 USC 103(a)

Claims 3-4 are rejected under 35 USC 103(a) as being unpatentable over Golke in view of Rockett (U.S. Patent No. 6,369,630). Applicant believes that the present amendments to Claim 1 overcome the rejections of Claims 3-4.

Conclusion

No new matter has been introduced by any of the above amendments. All claims should be now be in condition for allowance and a Notice of Allowance is